**In Lab Task:**

Implementation in Xilinx

module gate(a, b, c, d, e, f, g, h);

input a, b;

output c, d, e, f, g, h;

and (c, a,b); or (d, a,b);

nand (e, a,b);

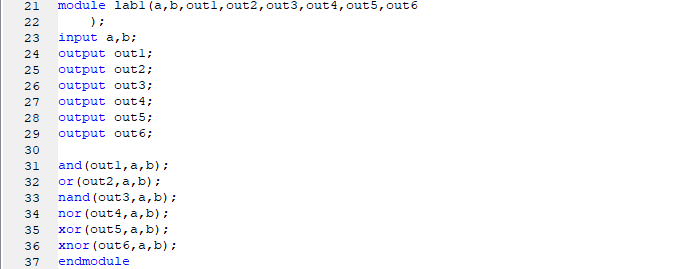
nor (f, a,b);

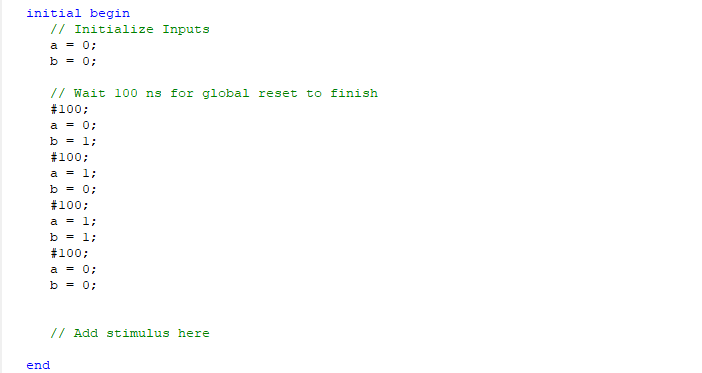
xor (g, a,b);

xnor (h, a,b);

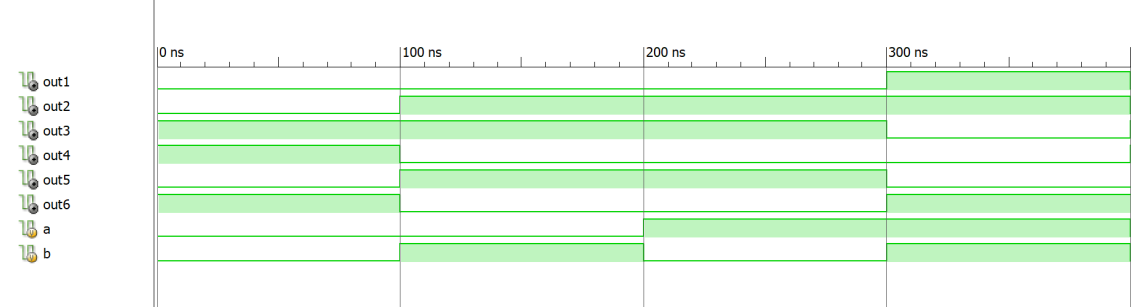
endmodule

**Code:**

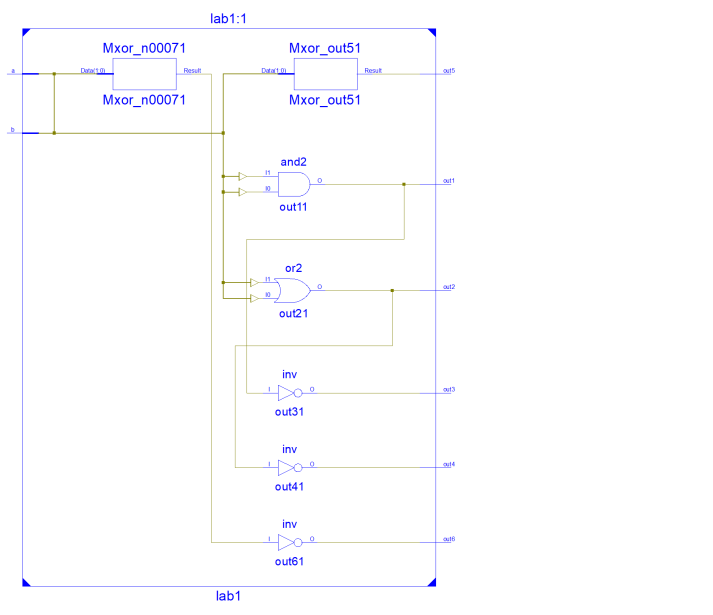




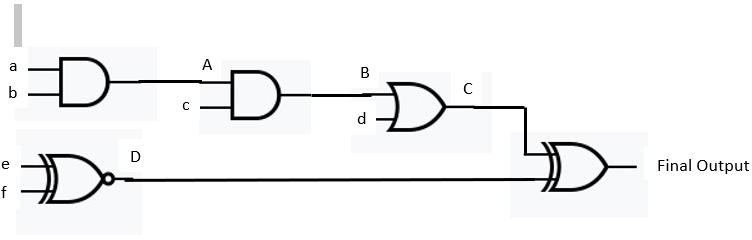
**Simulation:**



**Block Diagram:**



**Post Lab:** : Implement the following logic circuit in Xilinx ISE Design Suite. Also write test bench to verify your results. At the end, compare your results with Truth table.

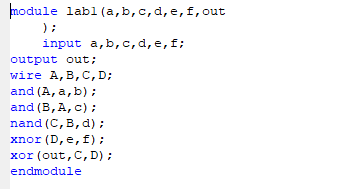


**Solution:**

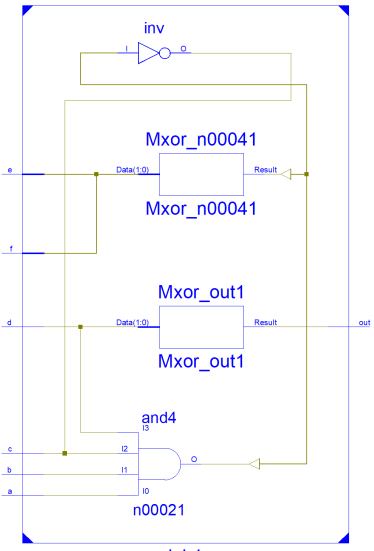
Truth table:

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| a | b | A | c | B | d | C | e | f | D | F |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

**Code:**



**Block Diagram:**



**Simulation:**

